MODULUS Ptolemy

Hardware Software Interface Document

Document: RO-LPT-OU-TN-3401

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CHANGE RECORD

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27th March 2000	Draft 5	draft
4th May 2000	Draft 6	draft
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11th September 2000	2.2 - RF freq. DAC added 2.9 – Corrections and clarification for docking station motor drive bits 2.10 – some analogue channel assignments changed. pressure sensor sensitivites changed to reflect 2.5V operation. Units column removed	3.1
19th March 2001	Changes to pressure sensors Revised calibration for docking station position monitor	4.0
3rd April 2001	2.10 - Revised conversions and shift counts for some HK analogue parameters. esp. pressure sensors.	5.0

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Ptolemy Hardware/Software Interface Document

Issue: 5

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CONTENTS

INTRODUCTION

This document describes the hardware/software interface for the electronics box controlling the Ptolemy experiment on the Rosetta Lander. All hardware registers are memory mapped

1.1 Definitions, acronyms and abbreviations

1.1.1 Definitions

Bit numbering:

Bits are numbered with the least significant bit as bit 0 and most significant bit as bit 15. This is the numbering used in the HS-RTX-2010RH processor reference manual, in the schematics for the electronics and in other hardware documents:

ms															ls
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

It should be noted that the software documentation (URD, SDD), numbers bits in the reverse order (most significant bit is bit 0, least significant bit is bit 15) as is usual with space data systems.

Instrument/Experiment:

As Roland is, itself, considered to be an instrument of the Rosetta spacecraft, this document refers to Ptolemy as an “experiment” or “subsystem”

1.1.2 Acronyms

ADC	Analogue to Digital Converter
ASIC	Applications Specific Integrated Circuit (i.e a custom chip)
CDMS	Command and Data Management System (Lander on-board computer)
DAC	Digital to Analogue Converter
FPGA	Field Programmabel Gate Array (such as the ACTEL chip on processor card)
HK	House Keeping - telemetry required to confirm correct operation of instrument
HT	High Tension (high voltage - ~2kV in this case)
HV	High voltage (same as HT)
I2C	Inter-IC - a serial bus protocol for transfering data between ICs.
IC	Integrated Circuit
MIPS	Millon Instructions Per Second
MORSP	Modulus On-board Real-time Software (Ptolemy)
OU	Open University
PWM	Pulse Width Modulation
RAL	Rutherford Appleton Laboratory
RICA	Rosetta Ion-Counter ASIC – one of the ASICs used to control & read the Ion-trap
SCIF	Space Craft Interface – FPGA that controls interface with the Lander CDMS
TC	Telecommands
Tlm	Telemetry
TM	Telemetry
VCO	Voltage Controlled Oscillator
WGA	Waveform Generator ASIC – the other ASIC used to control & read the Ion-trap

1.2 References

1.2.1 Applicable Documents

AD1		REID-A
AD2	ESA PSS 05	Software Engineering Standards
AD3	BSC(96)2 issue 1	Guide to applying PSS 05 to small software projects

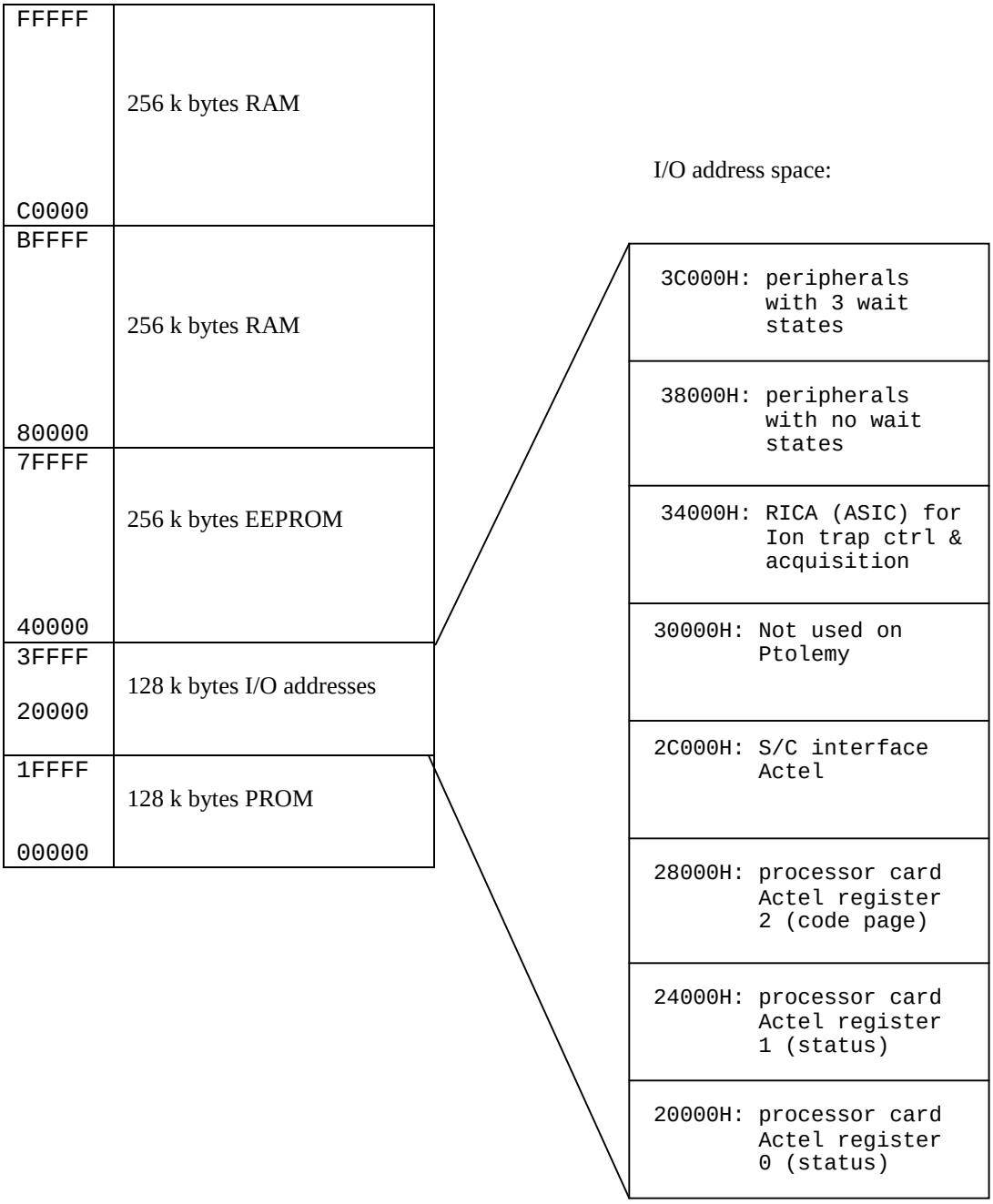
1.2.2 Reference Documents

RD1	RO-PTO-RS-0001/EID B	REID-B
RD2		Ptolemy Operations Plan
RD3	RO-BER-RAL-TN-3401	WGA and RICA applicability to RF Scan Function Design

2. PROCESSOR MEMORY MAP

2.1 Overview

The overall memory map for the electronics box is shown below. The total address space is 1048576 bytes (a 20 bit address bus) This comprises 16 pages each of 65536 bytes. The first 2 pages of memory are occupied by fuse-link PROM (containing the baseline flight software) and the top 8 pages are static RAM for variables and copied program code. Above the fuse-link PROM are two pages allocated to I/O registers and, above these, 4 pages (4,5,6 & 7) occupied by EEPROM and are intended for storing patches and updated tables.



2.2 Map of I/O pages

The table below shows an overall map of the I/O pages. All I/O registers are at even addresses and should be accessed with a word read or write instruction, even if they have no meaningful bits in the upper byte.

Addr range	Description	Address format (binary)
20000-23FFE	Low byte of processor card status register	0010 00xx xxxx xxxx xxx0
24000-27FFE	High byte of processor card status register	0010 01xx xxxx xxxx xxx0
28000-2BFFE	Processor board page register	0010 10xx xxxx xxxx xxx0
2C000-2FFFE	SCIF – Lander interface FPGA	0010 11xx xxxx xxxx xss0
30000-33FFE	Not used for Ptolemy	0011 00xx xxxx xxxx xxx0
34000-37FFE	RICA (Ion trap control)	0011 01xx xxxx xxrr rrr0
38000-3BFFE	Other peripherals with no wait states:	0011 10-- ---- ---- ----
38000-3800E	Telemetry channel select (W)	0011 10xx xxxx 0000 xxx0
38010-3801E	Trigger ADC (W)	0011 10xx xxxx 0001 xxx0
38020-3802E	ADC result register (R)	0011 10xx xxxx 0010 xxx0
38080-3808E	Not used	0011 10xx xxxx 1000 xxx0
38090-3809E	DAC enable register	0011 10xx xxxx 1001 xxx0
380A0-380AE	Valve data (on/off) register	0011 10xx xxxx 1010 xxx0
380B0-380BE	Valve data (on/off) enable register	0011 10xx xxxx 1011 xxx0
380C0-380CE	PWM data register	0011 10xx xxxx 1100 xxx0
380D0-380DE	PWM enable register	0011 10xx xxxx 1101 xxx0
380E0-380EE	Critical functions register	0011 10xx xxxx 1110 xxx0
380F0-380FE	Critical functions enable register	0011 10xx xxxx 1111 xxx0
3C000-3FFFE	Peripherals with 3 wait states	0011 11-- ---- ---- ----
3C070-3C07E	Set RF Frequency DAC	0011 10xx xxxx 0111 xxx0
3C080-3C08E	DAC chan/data register	0011 11xx xxxx 1000 xxx0

xx… - don't care; the read shall access the same register whatever the contents of this field
ss - this bit field selects an internal register in the SCIF FPGA
rrrrr - this bit field selects an internal register in the RICA ASIC

The 3-wait state option is only forseen for writes to the DAC chan/status register and the RF frequency DAC. For these registers 3 wait states are mandatory and the address 3C0XX should always be used instead of 380XX

2.3 Processor card status & page registers

The processor card status is contained in a 16 bit register in the processor card FPGA. Because, to save pins, only the low 8 bits of the data bus are connected to the processor card FPGA, this register is implemented as two 8 bit registers (plus a 4 bit register for saving the code page) at addresses 20000H (0010 00xx xxxx xxxx xxx0) for the low byte and 24000H (0010 01xx xxxx xxxx xxx0) for the high byte (and 28000H or 0010 10xx xxxx xxxx xxx0 for the code page register).

MS bit	Processor status low byte (20000H)						Ls bit
7	6	5	4	3	2	1	0
INH1 (R)	SW NMI #2 (R/W)	SW NMI #1 (R/W)	EEPROM ready (R)	Current trip (R)	Wdog NMI (R/W)	SW sys. Reset (R/W)	SW proc. Reset (R/W)

MS bit	Processor status high byte (24000H)						Ls bit
7(15)	6(14)	5(13)	4(12)	3(11)	2(10)	1(9)	0 (8)
Spare (R0)	Spare (R0)	EEPROM Int clear R(1)/W	EEPROM protect (R/W)	I-trip int clear R(1)/W	Wdog restart R(0)/W	Spare R(0)	INH2 (R)

R - read only
R(0) - always reads 0
R(1) - always reads 1
R/W - read/write
SW - software

The functions of the bits defined above are described in the following table:

Bit/ word	Bit/ byte		**Function**
			High byte
15	7	Spare (R0)	This bit is not currently used and always reads as 0
14	6	Spare (R0)	This bit is not currently used and always reads as 0
13	5	EEPROM Int clear R(1)/W	The software should write a 0 to this bit to clear the "EEPROM ready" interrupt (EI4). The bit always reads 1
12	4	EEPROM protect (R/W)	= 0: EEPROM disabled; reading and writing to EEPROM is prevented = 1: EEPROM enabled; reading allowed. Writing allowed provided correct pattern is sent to enable it.
11	3	I-trip reset R(1)/W	The software should write a 0 to this bit to clear the current trip maskable interrupt, EI5 (and the current trip flag in bit 3). This bit always reads 1
10	2	Wdog restart R(0)/W	The software should write a 1 to this bit to restart the watchdog timer. If it fails to do this within 1s of the previous restart (or power-on) the watchdog NMI is invoked. After a further 1s the watchdog reset is invoked.
9	1	Spare R(0)	This bit is not currently used and always reads as 0
8	0	INH2 (R)	This bit reflects the state of the Chemistry set inhibit 2 signal.
			Low byte
7	7	INH1 (R)	This bit reflects the state of the Chemistry set inhibit 1 signal
6	6	SW NMI #2 (R/W)	This bit may be set by the software to generate an NMI. The NMI condition shall be cleared by hardware on interrupt acknowledge but the bit shall remain set until reset or until cleared by software.
5	5	SW NMI #1 (R/W)	This bit has the same function as bit 6
4	4	EEPROM ready (R)	This bit reads 1 when the EEPROM is ready for writing (has completed a previous write). It goes to 0 when an EEPROM write is initiated.
3	3	Current trip (R)	This bit is set when a current trip interrupt is requested. This also initiates external interrupt 5 which may be cleared by writing 0 to bit 11.
2	2	Wdog NMI (R/W)	This bit is set to 1 by the hardware to indicate that a watchdog NMI has occurred. The software may clear this bit by writing a 0 to it.
1	1	SW sys. Reset (R/W)	The processor writes a 1 to this bit to assert the system reset. This pulls low a reset line to all boards on the backplan except the processor card. The software releases the reset by writing a 0 to this bit.
0	0	SW proc. Reset (R/W)	The software may reset the processor card by writing a 1 to this bit. The processor shall then be restarted. This bit shall remain at 1 and must be cleared before a further reset can be generated in this way.

The Processor card page register is a 4 bit read/write register that is intended to be used by the flight software to store the current program memory page number. Writing a value to this register does not, however, directly affect the addressing of memory; it is purely a storage location.

The register has the following format:

MS	Processor Card Page Register (28000H)															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
U	U	U	U	U	U	U	U	0	0	0	0	page (0-15)				

U – undefined; these bits shall probably contain the last value to be placed on the data bus. As the processor card FPGA is not connected to the high 8 bits of the data bus, it cannot force these bits to zero.

2.4 SCIF (Lander interface)

The SCIF is an FPGA on the Ptolemy backplane that handles the TC/TM interface between the ptolemy processor card and the Lander CDMS. It has the following registers:

Addr	Address format (x -> don't care)	R/W	Description
2C000	0010 11xx xxxx xxxx x000	Read	Interrupt Register
2C002	0010 11xx xxxx xxxx x010	Read	Status register (TC/TM status)
2C004	0010 11xx xxxx xxxx x100	Read	Received data register (TC data)
2C006	0010 11xx xxxx xxxx x110	Read	Not used
2C000	0010 11xx xxxx xxxx x000	Write	Not used
2C002	0010 11xx xxxx xxxx x010	Write	Status register (TC/TM status)
2C004	0010 11xx xxxx xxxx x100	Write	Not used
2C006	0010 11xx xxxx xxxx x110	Write	Transmit data register (TM words)

2.4.1 Interrupt register

The low 3 bits of the interrupt register show the status of the three interrupt sources. The upper 13 bits always read 0:

MS	Interrupt Register (32C000H)															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	C	B	A	

The interrupt sources are as follows:

Source	Mode	Description
A	Any	When set, indicates the arrival of an Address word synchron. The received data register (at address 2C004H) contains the address word that caused the interrupt request.
B	Receive	When set, indicates the arrival of a CMD/data synchron while the interface was selected and was in receive mode. The received data register (at address 2C004H) contains the received command word.
C	Receive	When set, indicates the arrival of a Status synchron. The status register (address 2C002H) has been copied and is being transmitted.
C	Transmit	When set, indicates the arrival of a data synchron. The telemetry data register (address 2C006H) has been copied and is being transmitted. The next TM data word may now be written.

When one or more of the above events occur, an external interrupt 2 (EI2) is generated. Reading the interrupt register clears the interrupt request and sets A, B and C back to 0. The EI4 handler, after reading the interrupt register to acertain the source(s) of the interrupt, should check each of bits A, B and C and take the appropriate action in case of any one of them being set.

2.4.2 Status register

This is a read/write register holding the interface communications status. Most of the bits are hard wired to 0 or 1 and always read the same:

MS	Status Register (2C002H)														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	ME	CE	SR	1	0	0	0	BSY	SM	0	0

The following bits are significant:

10	ME	Message Error flag. The software should set this flag to 1 if it receives a subsystem address word with an illegal function code
9	CE	Count Error flag. The software should set this flag to 1 if it receives a message whose length does not agree with the value given in the SSADR word
8	SR	The software sets this bit to indicate that it has a service request to the CDMS. It should clear the flag once the CDMS has responded with a “send request” message.
3	BSY	Busy flag. The software sets this to indicate that it is unable to comply with a CDMS request. Use to be avoided if possible – not planned for Ptolemy.
2	SM	The software may set this flag to indicate that it is in sleep mode. Use not planned for Ptolemy

The status word is automatically transmitted by the hardware on receipt of a “send status” synchron from the CDMS. Such a synchron is sent at the end of each command message and at the end of each HK request. In order for the status word transmitted to reflect the up-to-date status of the interface, the status must be updated within 38μs of receiving an address word or a command word.

2.5 RICA

The RICA appears at address 34000H (more exactly, in all the 64 byte windows from 34000H to 37FC0H). The RICA contains 32 word addresses, 24 of which are used. The registers have even addresses (address bit 0 should always be 0).

Addr	Name	R/W	Description
34000	FIFO_Port_1	Read	Read low word (bits 15:0) from FIFO, word removed from FIFO
34002	FIFO_Port_2	Read	Interrogative read bits 25:16 of FIFO data + valid & error flags
34004	FIFO_Port_3	Read	Reads FIFO how full (10 bit count) + empty and full flags
34006	FIFO_Port_4	R/W	Read or write pattern to/from FIFO flip register bits 15:0
34008	FIFO_Port_5	R/W	Read or write pattern to FIFO flip register bits 30:16
3400A	FIFO_Port_6	Read	Reads FIFO vector bits 4:0
3400C	FIFO_Port_7	Write	Write test data (bits 5:0), test count (bits 9:0)
3400C	FIFO_Port_7	Read	Read test count (9:0) + flags: test complete, success, failure
3400E	FIFO_Port_8	Read	Read code bits (15:0) for test_mux=0, bits(30:16) for test_mux=1
34010	I2C_Port_1	Write	Write data to I2C transmit register (16 bit word)
34010	I2C_Port_1	Read	Permanent read from I2C receive register (16 bit word)
34012	I2C_Port_2	Read	Interrogative read from I2C receive register
34014	Soft_Ctl_Port	R/W	Set/clear/read software resets and test controls
34016	DACC_Port	R/W	RICA DAC o/p bits (11:0) write or read back
34018	RFClk_Port_1	R/W	8 bit divider for RF clock (not used for Ptolemy)
3401A	RFClk_Port_2	R/W	8 bit divider for tickle clock (not used for Ptolemy)
3401C	Wdog_Port	R/W	Read/Write the RICA watchdog (no use planned for Ptolemy)
3401E	Not used		
34020	Exp_Port_B_0	Write	Expansion port 0 – write 16 bits to exp bus with decode 0 active
34022	Exp_Port_B_1	Write	Expansion port 1 – write 16 bits to exp bus with decode 1 active
34024	Exp_Port_B_2	Write	Expansion port 2 – write 16 bits to exp bus with decode 2 active
34026	Exp_Port_B_3	Write	Expansion port 3 – write 16 bits to exp bus with decode 3 active
34028	Exp_Port_B_4	Write	Expansion port 4 – write 16 bits to exp bus with decode 4 active
3402A	Exp_Port_B_5	Write	Expansion port 5 – write 16 bits to exp bus with decode 5 active
3402C	Exp_Port_B_6	Write	Expansion port 6 – write 16 bits to exp bus with decode 6 active
3402E	Exp_Port_B_7	Write	Expansion port 7 – write 16 bits to exp bus with decode 7 active
34030	Ion_Port_1	R/W	Read/Write contents of ion-counter 1 (diagnostic only)
34032	Ion_port_2	R/W	Read/Write contents of ion-counter 2 (diagnostic only)
34034	Chan_port	R/W	Low 10 bits hold channel count, incremented by chan_inc
34036-3403E	Not used		

2.5.1 FIFO_Port_1 – FIFO low 16 bits permanent read

This is a read-only port that returns the low 16 bits of the next word from the FIFO. The 26 bit count/channel number is then removed from the FIFO. In order not to loose bits 25:16 of the FIFO entry, these should be read from FIFO_Port2 before reading bits 15:0 from FIFO_Port_1

MS	FIFO_Port_1(34000H) Read															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	

This word contains the counts for an element of an ion-trap spectrum. Bit 15, once set remains at 1 as an indication that the count has overflowed the lower 15 bits.

2.5.2 FIFO_Port_2 – FIFO high bits and flags interrogative read

This is a read-only port that returns the following data:

MS	FIFO_Port_2 (34002H) Read														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FV	FIFO error				0	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

Where:

FV	FIFO_validB - should be 0 for valid data	
FIFO error	FIFO error bits should be all 0	x1xx – FIFO has fewer words that indicated by count 1xxx – FIFO has more words than indicated by count
Bit 10	Always 0	
D25-D16	This field contains the top 10 bits of the next 26 bit value in the FIFO. This corresponds to the channel number for the count in FIFO_Port_1	

Before reading FIFO_Port_1, this port should be read to get bits 25-16 (top 10 bits) of the 26 bit count+channel entry. Bits 10 to 15 of this word (top 6 bits) should be 0, any other combination constitutes an error.

2.5.3 FIFO_Port_3 FIFO full/empty status

This is a read-only port that reports the state of the 26-bit-wide FIFO:

MS	FIFO_Port_3 (34004H) Read														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE	FF	0	0	0	0	FIFO_howFull									

FF - FIFO full flag. =1 if FIFO is full, =0 if FIFO is not full
FE - FIFO empty flag. =1 if FIFO is empty, =0 if FIFO is full
FIFO_howFull - FIFO contents count – count of number of entries remaining in FIFO (0-1023)

2.5.4 FIFO_Port_4 FIFO flip bits 15:0

This read-write register allows the software to set and read the lower 16 bits of the 31-bit FIFO flip register. This may be used to corrupt deliberately the contents of the FIFO for test purposes.

MS	FIFO_Port_4 (34006H) Read/Write														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO flip bits 15:0															

2.5.5 FIFO_Port_5 FIFO flip bits 30:16

This read-write register allows the software to set and read the upper 15 bits of the 31 bit FIFO flip register.

MS	FIFO_Port_5 (34008H) Read/Write														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	FIFO flip bits 30:16														

Bit 15 is not used and always reads 0. Bits 14:0 control FIFO flip bits 30:16.

2.5.6 FIFO_Port_6 FIFO vector

This read-only register allows the software to read the FIFO vector, a 5 bit value

MS	FIFO_Port_6 (3400AH) Read only															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	FIFO vector					

2.5.7 FIFO_Port_7 Test data/Test count/Test result

This is a read/write register. The software writes test data to bits 15-10 and the test count to bits 9-0:

MS	FIFO_Port_7 (3400CH) Write															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Test data						Test count										

The test count and test result can be read from the same address:

MS	FIFO_Port_7 (3400CH) Read															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
TC	TS	TF	0	0	0	Test count										

TC - Test complete – set when test is complete
TS - Test success – set if test was successful
TF - Test fail – set if test failed

2.5.8 FIFO_Port_8 read code

This read-only register allows the software to read the 31 bit code. Bits 15:0 are read if the test_mux field is 0. Bits 30:16 are read if the test_mux field is 1. The test_mux bit is in the Softt_Ctrl_Port register.

MS	FIFO_Port_8 (3400EH) Read (test_mux=0)															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
code bits 15:0																

MS	FIFO_Port_8 (3400EH) Read (test_mux=1)															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	Code bits 30:16															

2.5.9 I2C_Port_1 – read/write I2C data

This Port allows data to be written to the I2C port for transmission, received data to be read from the I2C port and the status of the I2C port to be read

Writing a byte to I2C_Port_1 causes it to be transmitted via the I2C interface:

MS	I2C_Port_1 (34010H) Write															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Not used							lbyt	Transmit data								

The bit lbyt (bit 8) is set by the software to indicate the last byte of a message.

Reading a byte from I2C_Port_1 removes a data byte from the received data field (if any) and returns the interface status:

MS	I2C_Port_1 (34010H) Read														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used					abrt	rcv ept	tx free	Received data byte							

Bits	Desg	Description
15:11	Not used	Unused bits
10	abrt	If set, operation aborted
9	rcv ept	If set, the receive data register is empty (no new receive data)
8	tx free	If set, the transmit register is free (next byte of data may be written)
7:0	Received data	Last received byte

This read of the received data register is destructive, after the read, the next byte of received data may replace the contents of the receive register.

2.5.10 I2C_Port_2 – non-destructive read of I2C received data

This is a non-destructive read, the data remains in the receive register, reception of further words is not enabled. This address should be used to check on the interface status.

MS	I2C_Port_2 (34012H) Read														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used					abrt	rcv ept	tx free	Received data byte							

2.5.11 Soft_Ctrl_Port

This read/write port allows the software to reset and configure various RICA functions.

MS	Soft_Ctrl_Port (34014H) Read/Write														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	Wd rs	Tst Mx	Tst m2	Tst m1	Ct rst	Fif rst	I2c rst

Bit	Desg.	Function	
15:7	0	Not used – read as 0	
6	Wd rs	Set to reset on-chip watchdog timer – not used on Ptolemy	
5	Tst mx	Test_mux	=0: FIFO_Port_8 reads bits 15:0 of 31 bit FIFO code =1: FIFO_Port_8 reads bits 30:16 of 31 bit FIFO code
4	Tst m2	When set, selects test mode 2	
3	Tst m1	When set, selects test mode 1	
2	Ct rst	Writing a zero to this bit asserts the count reset, writing a 1 releases it	
1	Fif rst	Writing a zero to this bit asserts the FIFO reset, writing a 1 releases it	
0	I2c rst	Writing a zero to this bit asserts the I2C reset, writing a 1 releases it	

2.5.12 DACC_Port – DAC counter port

This read/write port allows software acces to the DAC counter port. This value is output as a 12 bit parallel signal for conversion by a DAC to control the RF signal amplitude. The DAC value can be incremented or decremented by pulses from the WGA without software intervention

MS	DACC_Port (34016H) Read/write															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	Current DAC value												

2.5.13 RFClk_Port_1 – RF clock generator I/F port 1

This read/write port allows the software to set and read back the divider that controls RF clock 1. The RF frequency shall be 4194304 Hz divided by the value in RFClk_Port_1 This register is not used to control the Ptolemy RF clock – a VCO circuit is used that gives better resolution.

MS	RFClk_Port_1 (34018H) Read/write															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	RF clock 1 divider									

2.5.14 RFClk_Port_2 – RF clock generator I/F port 2 – tickle clock

This read/write port allows the software to set and read back the divider that controls RF clock 2. The RF tickle frequency shall be 4194304 Hz divided by the value in RFClk_Port_2 This is not used on Ptolemy as the tickle signal has been removed from the design:

MS	RFClk_Port_1 (34018H) Read/write															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	RF clock 2 divider									

2.5.15 Assignment of WGA outputs

The WGA is programmed via the RICA I^2C interface. Details of the WGA operation are described in RD3. Specific to Ptolemy, however, are the following bit assignments for WGA outputs:

WGA bit	Function
0 (LS bit)	Incremnet Ring RF (DAC_up)
1	Decrement Ring RF (DAC_Down)
2	Increment Channel Number (Chan_inc)
3	Extractor/Nanotip
4	Electron Repeller/Gate2
5	-
6	-
7	Ion_trap_inp2

2.6 DC DAC outputs

The DC DAC is used to set each of the DC voltage levels required to operate the various items in the science system. The RF amplitude voltage is set via a separate DAC, controlled by the WGA via the RICA.

2.6.1 The DAC output/channel select register

To set the output level for one of the DACs, the software shall write a 16 bit word to the port at address 3C080H containing the 8 bit value to output and the 4 bit address of the channel to be set:

MS	DC DAC control (3C080H): Write															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
DAC o/p value (0-255)								not used				DAC chan sel (0-15)				

After writing a value to the DC DAC control register, it is recommended to wait ~1ms (TBC) before writing a subsequent value (i.e for a different DAC channel) to allow time for the current channel to charge.

In order to maintain the output voltage of a channel constant to within ± 1 lsb, it is recommended that each channel be refreshed (re-written) no less frequently than every 64ms (TBC).

2.6.2 DAC channel enables

This 16 bit register shall be implemented with an enable/disable bit for each analogue channel

MS	DC DAC enable register (38090H) Write															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
spr	c14	c13	c12	c11	c10	c09	c08	c07	c06	c05	c04	c03	c02	c01	c00	

cnn enable/disable bit for channel nn bit set for enable, reset for disable
spr spare channel enable/disable bit

The DC DAC channel enable registers shall be initialised to 0 at power-on (all channels disabled) but the software should also write zeros to these registers as part of safe-mode initialisation as a precaution against possible failure of initialisation by the FPGA.

2.6.3 DC DAC channel assignments

The channels are assigned to analogue outputs as follows:

Chan	**Description**	**1 DAC lsb**	**remarks**
00	Ion Trap DC control 1 (extractor voltage)		
01	Ion Trap DC control 2 (electron gate 1 voltage)		
02	Ion Trap DC control 3 (electron repeller voltage)		
03	Ion Trap DC control 4 (electron gate 2 voltage)		
04	Nanotip current		
05	HT (2.5kV) voltage		
06	Docking station DC motor drive upper position		see 2.9.3
07	Docking station DC motor drive lower position		see 2.9.3
08	hLV1 – Lindau valve LV1 heater		
09	hLV2 – Lindau valve LV2 heater		
10	deleted		was LV3 heater
11	deleted		was LV4 heater
12	hLV5 – Lindau valve LV5 heater		
13	hLV6 – Lindau valve LV6 heater (formerly RV1)		
14	hLV7 – Lindau valve LV7 heater (formerly RV2)		
15	Spare		

Channels 6 and 7 are used to set target (limiting) postitions when driving the docking station. The motor drive shall fall to 0 when the target position is reached or passed. This reduces the timing demands on the flight software when operating the docking station.

2.7 PWM output channels

These digital (on/off) channels switch power to reactors and heaters. A 16 bit register at address 380C0H contains 1 bit for each output. Setting a bit to 1 shall switch on the corresponding output and setting a bit to 0 shall switch off the corresponding output. These Channels are intended to be used with software PWM – Each channel to be activated shall be assigned a time window in a repeating 0.25s (TBC) period. The heating effect shall be modulated by varying the period for which the channel is actually pulsed on within this window.

A second 16 bit register at location 380D0H shall contain an enable/disable bit for each output. Setting a bit in this register to 1 shall enable the corresponding output, setting it to 0 shall disable the corresponding output.

2.7.1 PWM output control register

MS	PWM O/P register (380C0H) Write														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
c15	c14	c13	c12	c11	c10	c09	c08	c07	c06	c05	c04	c03	c02	c01	c00

cnn on/off bit for channel nn bit set for on, reset for off
spr spare channel on/off bit

2.7.2 PWM output enable register

MS	PWM O/P enable register (380D0H) Write														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
c15	c14	c13	c12	c11	c10	c09	c08	c07	c06	c05	c04	c03	c02	c01	c00

cnn enable/disable bit for channel nn bit set for enable, reset for disable
spr spare channel enable/disable bit

2.7.3 PWM output channel assignments

Chan	**Description**	
00	Reactor R1 heater	
01	Reactor R2 heater	
02	Reactor R4 heater (reactor 3 deleted)	
03	Reactor R5 heater	
04	Reactor R6 heater	
05	Reactor R7 heater	
06	Reactor R8 heater	
07	Reactor R9/R14 heater	
08	Reactor R13 heater (reactors 10-12 deleted)	
09	Reactor R15 heater	
10	GC heater	
11	ENC1 Heater	
12	ENC2 Heater	
13	Ion Trap heater	
14	Transfer pipe heater	
15	Oven heater	

2.8 Digital (On/Off) channels

These channels appear to the software as simple on/off controls. Any pulse timing required shall be performed in hardware.

2.8.1 Digital (On/Off) output control register

MS	Digital (On/Off) O/P register (380A0H) Write														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
c15	c14	c13	c12	c11	c10	c09	c08	c07	c06	c05	c04	c03	c02	c01	c00

cnn on/off bit for channel nn bit set for on, reset for off

2.8.2 Digital (On/Off) output enable register

MS	Digital (On/Off) O/P enable register (380B0H) Write														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
c15	c14	c13	c12	c11	c10	c09	c08	c07	c06	c05	c04	c03	c02	c01	c00

cnn enable/disable bit for channel nn bit set for enable, reset for disable

2.8.3 On/Off channel assignments:

Chan	**Description**	
00	CV1	Clipard Valve
01	CV2	Clipard Valve
02	CV3	Clipard Valve
03	CV4	Clipard Valve
04	CV7	Clipard Valve
05	CV8	Clipard Valve
06	CV9	Clipard Valve
07	CV10	Clipard Valve
08	CV11	Clipard Valve (3-way)
09	CV13	Clipard Valve
10	CV14	Clipard Valve
11	CV15	Clipard Valve
12	CV16	Clipard Valve (3-way)
13	CVA	Injector control valve
14	CVB	Injector control valve
15	CVC	Injector control valve

2.9 Critical function channels

These channels control critical functions which could endanger instrument survivability if activated at the wrong time. Each of these functions has a corresponding enabable bit in the Critical functions enable register.

2.9.1 Critical functions register

MS	Critical functions register (380E0H) Write														LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
not used									MU	MD	HT	-	-	R2	R1

HT	Set to switch on the High Tension, nanotip and extractor supplies to the Ion-trap. These should only be activated when the instrument is in a vacuum.
R1-R2	Rupture valve outputs. To activate a rupture valve heater, the corresponding bit must be cycled between 0 and 1 with a frequency of not less than 8KHz (TBC).
MD	Motor Down drive enable – allows docking station motor to drive down (dock)
MU	Motor Up drive enable – allows docking station motor to drive up (undock)

2.9.2 Critical functions enable register

MS	Critical functions enable register (380F0H) Write															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
not used									MU	MD	HT	-	-	R2	R1	

HT, R1,R2, MU and MD represent enables for the 5 critical function channels. These bits must be set for the critcal function to operate.

2.9.3 Operation of the docking station.

To enable a docking station operation, the appropriate bit (MU or MD) must be set in the critical functions enable register (2.9.2, above).

To operate the docking station, the upper and lower docking station positions (DC DAC channels 6 &7 repectively – see 2.6.3) should first be set to the desired limits of travel. MD may then be set to start the docking station driving down or MU to start it driving up. When the docking station reaches the corresponding limit of travel (i.e is outside the range set by DC DAC channels 6 & 7), the motor shall be stopped by hardware intervention. When the software observes that the station has reached the desired position, or after an appropriate timeout, the software should reset the motor drive bit (MD for downward movement, MU for upward movement).

This scheme is intended to free the software from the need to check the docking station position with a high time resolution.

After a docking station operation, the motor drive enable bits (MU&MD) should be reset in the Critical functions enable register.

2.9.4 Rupture Valve operation

In order to protect the rupture valve function against latch-up of a single gate in the ACTEL, the heaters are driven by an AC coupled circuit which must be fed a square wave of frequency 8192 Hz (nominal). Thus, to keep the heater on, the software must flip the state of the appropriate bit (R1 or R2) every 61.025 μs (nominal) or 16384 times per second. This corresponds to a count of 256 in a 2010 timer register.

2.10 Analogue HK channels

To convert and acquire an analogue value, the software performs the following steps:

- Write the conversion address to the telemetry address register at 38000H
- Wait at least 100 μs for settling of the analogue signal
- Initiate conversion by a write (any value) to address 38010H
- Wait at least 20 μs for conversion
- Read the converted (digital) value from the 16 bit register at 38020H

The telemetry address channels are are 8 bit numbers and are assigned as shown in the following table:

TM channel		Description	Sensor Sensitivity	Electr-onics Gain	Sensivity at ADC i/p	HK Range of interest in Engineering units	ADC input voltage range	Nominal calibration for ADC units	Shift	Resolution in HK	Range available in HK ignoring sensor limits
Hex	Decimal							1 ADC lsb	→	1 lsb	
00	00	Reactor R1 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
01	01	Reactor R2 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
02	02	Reactor R4 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
03	03	Reactor R5 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
04	04	Reactor R6 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
05	05	Reactor R7 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
06	06	Reactor R8 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
07	07	Reactor R9 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
08	08	Reactor R13 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
09	09	Reactor R15 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
0A	10	Lindau valve LV1 t/couple (N-type)	26.1 µV/K	100	2.61mV/K	-100-200 °C	0-1.25V	0.117 K	4	1.88°C	±210°C
0B	11	Lindau valve LV2 t/ocouple (N-type)	26.1 µV/K	100	2.61mV/K	-100-200 °C	0-1.25V	0.117 K	4	1.88°C	±210°C
0C	12	spare differential input gain 100									
0D	13	spare differential input gain 100									
0E	14	Lindau valve LV5 t/couple (N-type)	26.1 µV/K	100	2.61mV/K	-100-200 °C	0-1.25V	0.117 K	4	1.88°C	±210°C
0F	15	Lindau valve LV6 t/couple (N-type) (was RV1)	26.1 µV/K	100	2.61mV/K	-100-200 °C	0-1.25V	0.117 K	4	1.88°C	±210°C
10	16	Lindau valve LV7 t/couple (N-type) (was RV2)	26.1 µV/K	100	2.61mV/K	-100-200 °C	0-1.25V	0.117 K	4	1.88°C	±210°C
11	17	GC thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-100-250 °C	0-1.25V	0.117 K	5	3.75°C	-273/+387°C
12	18	Manifold (Thermal enclosure) A t/couple (N-type)	26.1 µV/K	100	2.61mV/K	-100-200 °C	0-1.25V	0.117 K	4	1.88°C	±210°C
13	19	Manifold (Thermal enclosure) B t/couple (N-type)	26.1 µV/K	100	2.61mV/K	-100-200 °C	0-1.25V	0.117 K	4	1.88°C	±210°C
14	20	Ion trap thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-100-200 °C	0-1.25V	0.117 K	4	1.88°C	±210°C
15	21	Oven thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
16	22	Pipe heater thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-200-200 °C	0-1.25V	0.117 K	4	1.88°C	±210°C
17	23	Absolute pressure sensor G1 (KPY 44A)	15mV/bar	100	1.5V/bar	0-4 bar	0-10V	203.45 µbar	7	26.04 mbar	0-6.67 bar

18	24	Absolute pressure sensor G2 (KPY 45A)	6.5mV/bar	100	0.65V/bar	0-10 bar	0-10V	469.5 µbar	7	60.1mbar	0-15.38 bar
19	25	Absolute pressure sensor G3 (KPY 44A)	15mV/bar	100	1.5V/bar	0-4 bar	0-10V	203.45 µbar	7	26.04 mbar	0-6.67 bar
1A	26	Absolute pressure sensor G4 (KPY 43A)	22mv/bar	100	2.2V/bar	0-1.6 bar	0-5V	138.72 µbar	6	8.88 mbar	0-2.27 bar
1B	27	Absolute pressure sensor G5 (KPY 42A)	37.5mV/bar	100	3.75V/bar	0-0.6 bar	0-2.5V	81.38 µbar	5	2.604 mbar	0-0.67 bar
1C	28	Reactor R14 thermocouple (N-type)	26.1 µV/K	100	2.61mV/K	-273-1300 °C	0-10V	0.117 K	7	15°C	-273/+1300°C
1D-1F	29-31	3 unsused channels									
2X	32-47	reference junction thermometer (AD590) Kelvin!	10mV/K	1	10mV/K	-100-100 °C	0-5V	30.5176mK	6	1.95K	0-499K
3X	48-63	Docking Station					0-2.5V	1.587µm	5	50.8µm	0-13mm 0-2.5V
4X	64-79	Nanotip drive voltage	25V/V	1	25V/V	0-110V	0-5V	7.629mV	6	0.488V	0-125V
5X	80-95	Detector bias (HT)	1kV/V	1	1kV/V	0-5kV	0-5V	305.176mV	6	19.5V	0-5kV
6X	96-111	5V voltage monitor	1 V/V	0.5	0.5V/V	0-10 V	0-10V	610.352µV	6	39mV	0-10V
7X	111-127	28V voltage monitor	1V/V	0.1	0.1V/V	0-50V	0-5V	3.05176mV	6	195mV	0-50V
8X	128-143	5V current monitor	1A/V	1	1A/V	0-2A	0-2.5V	305.176µA	5	9.77mA	0-2.5A
9X	144-159	28V current monitor	1A/V	1	1A/V	0-2A	0-2.5V	305.176µA	5	9.77mA	0-2.5A
AX	160-175	RF calibration (monitors RF amplitude – see 2.11)	10mV/V	1	10mV/V	0-250V	0-2.5V	30.5176mV	5	0.977V	0-250V
BX	176-191	Spare channel									
CX-FX	192-255	not used									

X	Don't care; these bit fields are not decoded by the hardware it is suggeted that 0 be used.
TM channel	The channel number that must be written to the multiplexor to select this TM reading.
Units	The reading at the sensor corresponding to 1 ADC unit.
Nom. Cal	The nominal range corresponding to 1 lsb at the ADC (but some channels are non-linear)
Shift	Number of bits that the 16 bit value is shifted right before inclusion in the HK data
Res. in HK	The approximate resolution, in engineering units, for a single lsb in the HK data – Note that, in the Aux data, the full 16 bit resolution is available.
Pressure sens.	All pressure sensors have an exitation of 2.5V

The A/D converter provides a 16 bit 2's complement output corresponding to a volage range of –10V to +10V. The range of the ADC is as follows:

Input voltage	**ADC reading**	
	Hex	**Decimal**
-10V	8000	-32768
0V	0000	0
9.9997V	7FFF	+32767

One telemetry count corresponds to a voltage of 305.176μV at the input to the ADC. Many analogue channels have signal conditioning before the ADC which modifies this ratio.

2.10.1 Thermocouples and pressure sensors

The thermocouple/pressure sensor channels have an amplification stage with a gain of 100 before the ADC and so have a scale of 3.05176μV per telemetry count. At 0 °C, this corresponds to ~0.117K per ADC unit.

Before using the Thermocouple readings for temperature monitoring/control, the values must be corrected for the reference junction temperature. The necessary correction, in μV, is:

$$k_1*T+k_2*T^2+k_3*T^3$$

Where:

T is the reference junction temperature in °C
$k_1 = 25.95 \quad \mu VK^{-1}$
$k_2 = 0.015 \quad \mu VK^{-2}$
$k_3 = 0.0 \ \mu VK^{-3}$

This gives a result correct to ± 10μV within the temperature range -85°C to +65°C for the reference junction.

2.10.2 Reference junction temperature

This temperature is measured with an AD590 sensor providing 1μA per Kelvin. A 10KΩ resitor is used to convert this to a voltage input of 10mV(or 32.768 telemetry counts) per Kelvin

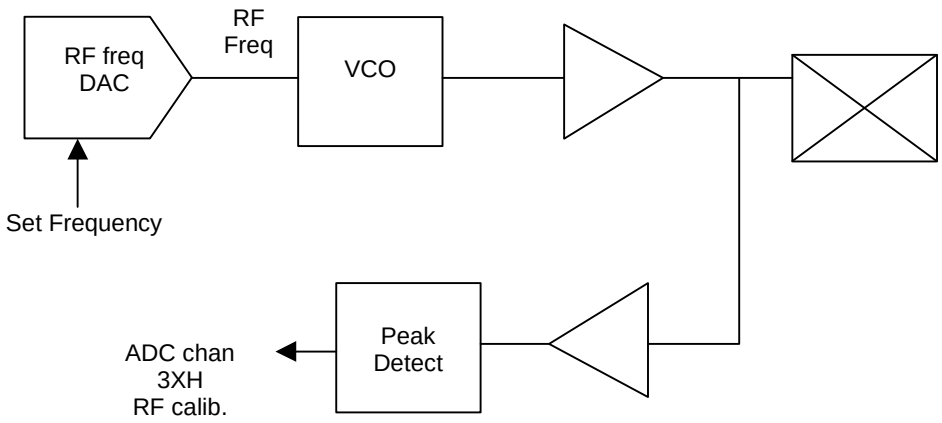
2.11 RF Frequency DAC

This DAC allows the software to set the frequency of the RF signal. It is separate from the other DAC channels described in 2.6 and does not require regular refreshes from the software. This is a 12 bit DAC taking an unsigned integer:

MS	Set RF Frequency DAC (38070H) Write															LS
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
unused				VCO control voltage												

The output from this DAC cotrols a VCO that feeds the RF generation circuit. By writing to this register the software can vary the RF frequency around a central value (for DAC contents= 800H)

The RF frequency DAC may be used, together with the RF calibration monitor (TM channel 3XH) to check or set the calibration of the RF amplitude.



By setting a scan function that produces a constant RF output and stepping the RF frequency DAC whilst reading the resulting RF signal from the RF calibration channel, it is possible to check the calibration of the RF circuit. It is possible that this calibration may drift over the mission lifetime.