Power Actuation and Switching Module DS1 Technology Validation Report

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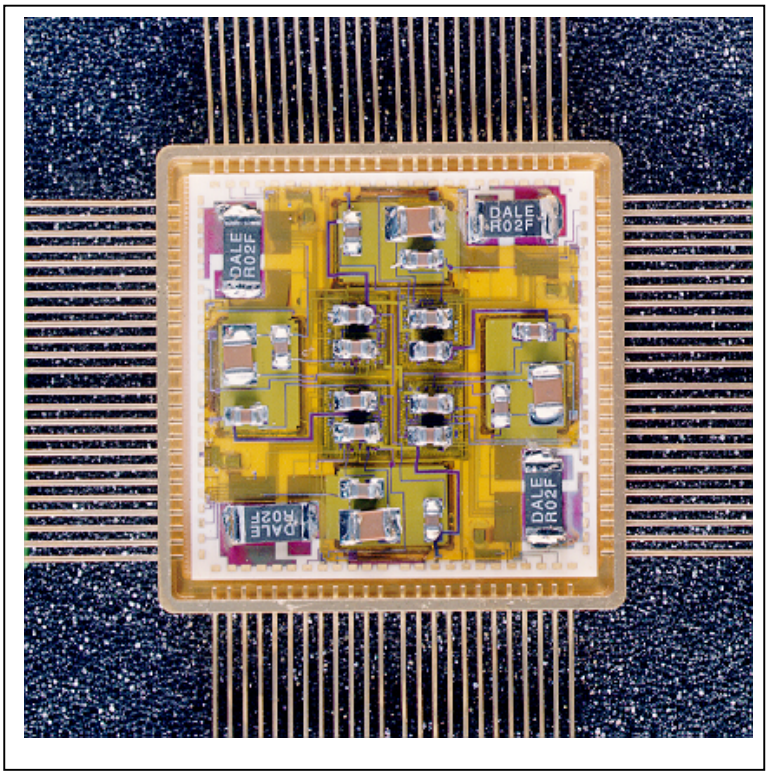

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EXTENDED ABSTRACT

In a unique JPL, Lockheed Martin, and Boeing government/industry partnership a "state of the art" power actuation and switching module (PASM) has been developed, designed, and fabricated for flight qualification on NASA's Deep Space 1 (DS1) mission in the third quarter of 1998. The features associated with the development of the PASM combine NASA/JPL's desire to advance the art of power electronics packaging, Lockheed Martin's proprietary high-density interconnect (HDI) technology, and Boeing Company's expertise in the application specific integrated circuit (ASIC) design and layout. The PASM development project was organized under JPL's New Millennium Program (NMP) Microelectronics Integrated Product Development Team (IPDT) and was cost-shared by both the government and industry. The industry assumed the cost of developing the product, and the government paid for its fabrication and test.

The PASM is a quad-switch device. Each of its four stand-alone switches provides the capability to switch power, to isolate faults, and to limit in-rush and fault currents, and supplies voltage and current telemetry. Additionally, it offers the capability for trip time control, di/dt and dv/dt control, and remote on/off control. Each switch can switch anywhere from 3 to 40 V at 3 A maximum and, as a result, can be used in switching the primary as well as the secondary side (conditioned) power. The use of HDI technology for packaging and ASICs for switch control electronics gives PASM a 4 to 1 weight, volume, and footprint advantage over existing hybrid products. It is the advanced packaging technology and utilization of ASICs that makes the PASM unique. It retains, with certain enhancements, all the electrical functions offered in a single-switch hybrid module.

Both HDI and mixed-signal ASIC technologies are rapidly maturing due to their applications in other power and non-power products as well as NASA's and the Air Force's commitment to continue to promote and enhance these technologies. These are strong product risk-mitigation steps that not only have helped to make PASM a successful product, but also have resulted in the successful development of credit card size dc-dc converters at Lockheed Martin.

The key purpose of the validation program was to validate the design and production processes for mixed signal ASICs and the HDI packaging technique and materials by exercising the electrical functions of the switches in the space environment. The validation program included flying two PASM modules as a Category 3 experiment on DS1. The test program included switching 5-V power to a 1-A resistive load through each of the eight switches (four per module). The switches were also operated in parallel (two at a time) to switch 5-V power to the same 1-A resistive load. Certain electrical design flaws in the switch control ASICs prevented them from operating completely. As a result, the in-rush and fault isolation features of the PASM switches were not tested.

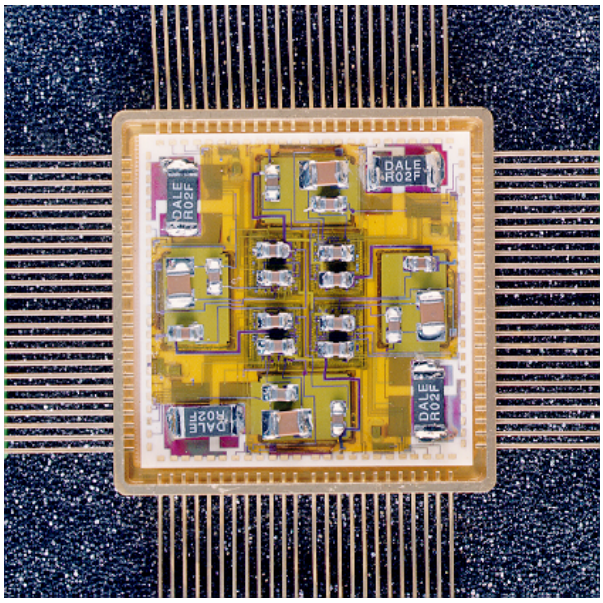
The PASM switches were successfully exercised several times during the mission and showed no performance degradation or inability to function.

NASA/JPL has recently awarded a second contract to the Boeing Company to produce a second-generation ASIC to correct the previous design flaws and simplify the design. These second-generation ASICs will be used in PASMs being procured by JPL for the X2000 program.

The PASM, as well as the technologies used in building it, have succeeded to a large extent in satisfying NASA's goal to miniaturize power electronics and provide wide-ranging applicability to future NASA science missions as well as other LEO and GEO spacecraft. Additional HDI products in development at Lockheed Martin include a second-generation PASM, dc-dc converters, shunt regulator modules, and lithium-ion battery chargers using PASM technologies. Many of these modules are slated to be delivered to JPL for NASA's X2000 programs in the near future.

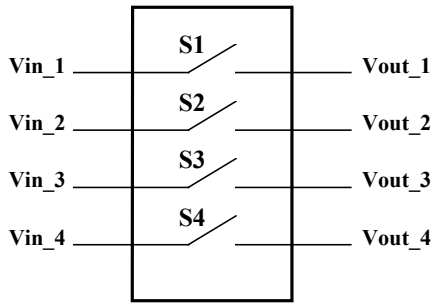
LOCKHEED MARTIN

Power Actuation and Switching Module (PASM) Fact Sheet



PASM Module (1.525" x 1.525" x 0.250")

Contact for additional product information:
Lockheed Martin Commercial Space Systems
Communications and Power Center
Newtown, PA 18940
215-497-1581
http://www.cpc.lmms.lmco.com



PASM Switch Configuration

What is it?

The power actuation and switching module (PASM) is a quad-switch module. Each of the four switches in the module operates as a circuit breaker by combining both the relay and fusing functions into a single device to safely switch electrical power to the spacecraft loads and to protect and isolate the power source from any load faults.

Why is it exciting technology?

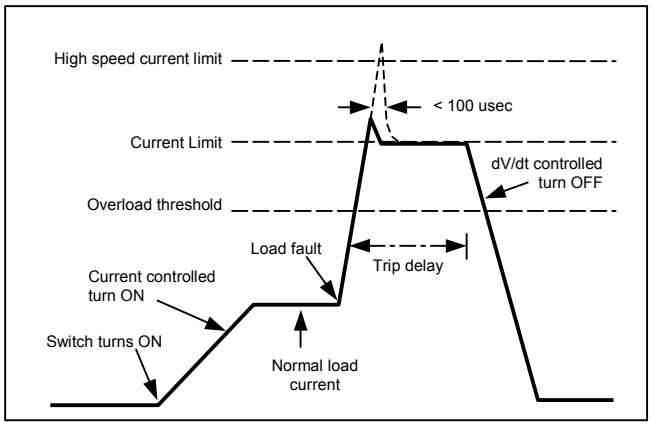
- Lower power hardware manufacturing and test costs
- >4× reduction in weight, volume, and footprint
- Enabling technology for small and large satellites
- Enabling technology for miniaturization of spacecraft power management and distribution modules

When will it be demonstrated?

- The flight demonstration on DS1 was completed in August 1999.
- The technology is being adopted by NASA/JPL X2000 program.
- The same packaging technique as well as the PASM are being used to produce other power modules such as dc-dc converters, shunt regulators, battery chargers, etc.

Who needs it?

- All space missions, as well as commercial consumer electronics and power supplies
- High-density power supplies, instruments, sensors, and micro-power systems or avionics modules.



Switch Current vs. Time

PASM Specifications

Parameter	Specification
Number of switches	four
Switched dc input voltage range (Vin)	3 V to 40 V (28 V nominal)
Housekeeping ± 15 V power (all switches off)	80 mW max.
Housekeeping ± 15 V power (all switches on)	600 mW max.
Rated switch current	3 A max.
Total switch current per module	12 A max. (sum of all four switches)
Switch on resistance (Vin to Vout)	85 mΩ (at 100 °C junction temperature)
Overload trip current	3.5 A ± 7%
Overload trip delay	500 µs min; 500 ms max.
Current limit	4.5 A ± 7%
Turn on time into full rated load	300 µs min; user select max.
Operational temperature range	–40 °C to +100 °C
Storage temperature range	–55 °C to +125 °C

Power Actuation and Switching Module Design and Development Flight Validation Report

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1.0 Introduction

The Power Activation and Switching Module (PASM) development project came about following the organization of the first two New Millennium Program (NMP) Microelectronics Integrated Product Development Team (IPDT) workshops in early 1996, where a road map for the development of multiple chip modules (MCMs) for power management and distribution (PMAD) electronics was identified. The IPDT industry members proposed various integration and packaging technologies to be developed or advanced jointly with the government, toward the goal of fabricating the MCMs for validation on various deep-space flights. The PMAD MCMs included the dc-dc converters, power regulation and control, and power-switching and distribution electronics. The PASM was conceived to be, and approved for development as the very first product toward fulfilling the NMP roadmap objectives. The Lockheed Martin Corporation's Missile and Space Division and the Boeing Company (the two key members of the microelectronics IPDT) put forth two separate proposals for the development of the PASM. The government (NASA/JPL) opted to combine the best parts of both proposals, thus forming a joint NASA/JPL, Lockheed Martin, and Boeing team for the development of the PASM. Lockheed Martin Corporation was given the overall program responsibility along with the fabrication of the flight-validation modules using their proprietary HDI (high-density interconnect) packaging technology. The Boeing Company was given responsibility for the development and fabrication of the application specific integrated circuits (ASICs) for the PASM. Most design and development effort was funded by the corporations' internal research and development funds, while the government paid for fabricating and testing modules, including the ASICs. The overall design and performance requirements for the PASM were defined by the Lockheed Martin Corporation. The Boeing Company was primarily responsible for the design of the control circuitry for the switch. Work on the production phase started in April 1997 and the flight-validation modules were delivered to JPL in September 1997. A picture of the fully finished de-lidded module is shown in Figure 1.

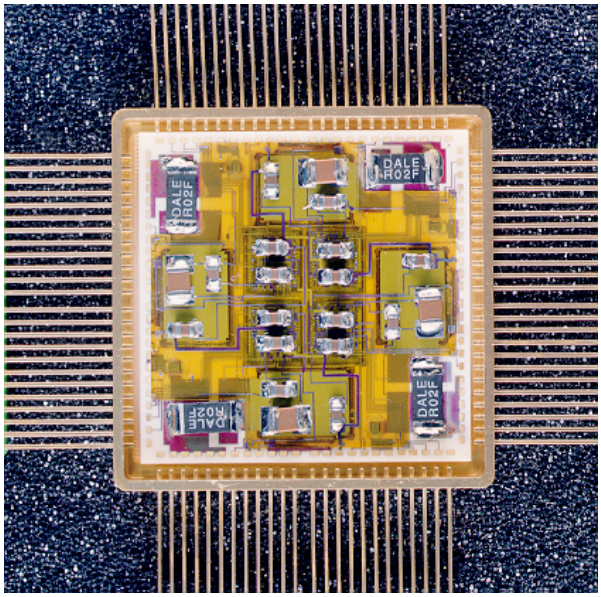

Figure 1. PASM Module (1.525 × 1.525 × 0.250 in.)

2.0 Technology Description

2.1 What It Is; What It Is Supposed To Do

The heart of each PASM is a switch control ASIC fabricated in Harris Semiconductor's Radiation-Hard Silicon Gate (RSG) process, which is radiation-total-dose tolerant and capable of sustaining high voltages. The PASM is a quad-switch device. Each of the four standalone switches provides the capability to switch power, isolate faults, and limit in-rush and fault currents. Each switch can switch anywhere from 3 to 40 V at 3 A maximum and, as a result, can be used in switching the primary as well as the conditioned (secondary) power. The PASM also includes trip-time control, di/dt control, and provides remote on/off capability and current and voltage telemetry. The use of HDI technology for packaging and of ASICs for switch control electronics gives the PASM a four-to-one weight, volume, and footprint advantage over existing products.

2.2 Key Technology Validation Objectives at Launch

The key purpose of the validation program was to validate the design and production processes for mixed signal ASICs and the HDI packaging technique and materials by

exercising the electrical functions of the switches in the space environment. The validation program included flying two PASM modules as a Category 3 experiment on DS1. The test program included switching 5-V power to a 1-A resistive load through each of the eight switches (four per module). The switches were also operated in parallel (two at a time) to switch 5-V power to the same 1-A resistive load. Certain electrical design flaws in the switch control ASICs prevented them from operating completely. As a result, the in-rush and fault isolation features of the PASM switches were not tested.

2.3 Expected Performance Envelope

The PASM switches were successfully exercised several times during the mission and showed no performance degradation or inability to function. Both the load voltage and current telemetry were monitored to assess the performance of each of the eight PASM switches and to ensure that the switch turn on voltage drop is not excessive.

2.4 Detailed Description

Electrical Design—A simplified functional block diagram of the PASM switch configuration is shown in Figure 2.

The module includes four independently configurable switches with independent command, telemetry, and housekeeping power lines. The only common node in the module is the ground. The switches either can be used individually or can be connected in series or in parallel externally for power switching. Each switch primarily functions as a fault isolation device or a circuit breaker and performs both power switching and fusing functions. It offers current controlled turn on (in-rush current limiting), fault current limiting, trip-time control, and voltage-controlled turn off. These features are graphically depicted in Figure 3.

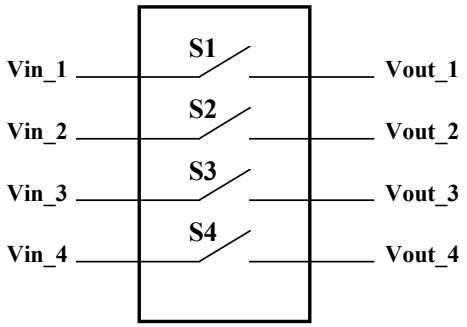

Figure 2. PASM Switch Configuration

The key performance parameters of the PASM are listed in Table 1. A more detailed functional diagram of a single switch in the PASM is shown in Figure 4, which shows the power-switch FET along with its SCA, various timing capacitors, current sense resistor, output clamp diode and associated input/output functions. Each of the four switches in the module includes a total of nine discrete components interconnected using the HDI technology.

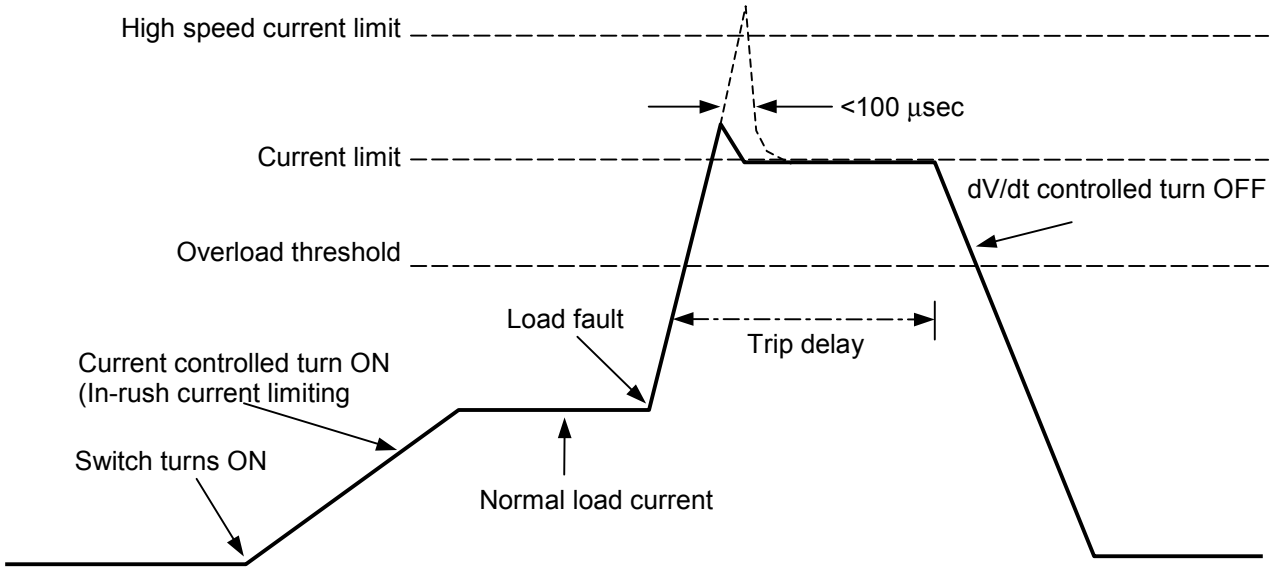

Figure 3. Switch Current vs. Time

Table 1. PASM Specifications

Parameter	Specifications
Number of switches	Four
Switched dc input voltage range (Vin)	3 V to 40 V (28 V nominal)
Housekeeping ±15 V power (all switches off)	80 mW max.
Housekeeping ±15 V power (all switches on)	600 mW max.
Rated switch current	3 A max.
Total switch current per module	12 A max. (sum of all four switches)
Switch on resistance (Vin to Vout)	85 mΩ (at 100 °C junction temperature)
Overload trip current	3.5 A ±7%
Overload trip delay	500 µsec min/500 msec max.
Current limit	4.5 A ±7%
Turn on time into full rated load	300 µsec min; user select max.
Operational temperature range	–40 °C to +100 °C
Storage temperature range	–55 °C to +125 °C

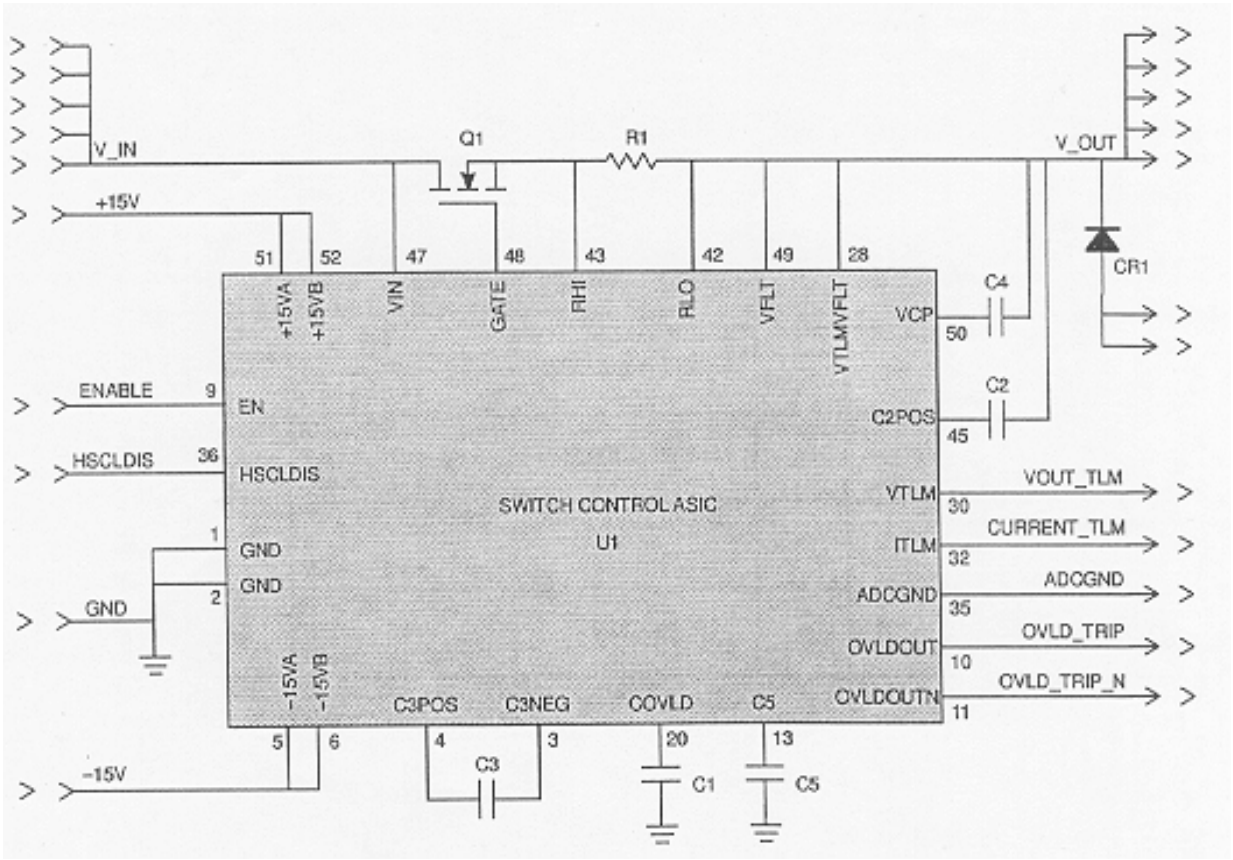

Figure 4. Detailed Functional Block Diagram (One of Four PASM Switches)

ASIC Design—The switch control ASIC (SCA) was custom designed by Boeing and fabricated in Harris Semiconductor's RSG process. The RSG process is thick-film SOI BICMOS with process enhancements to mitigate the threshold voltage shift post-radiation total dose. The SCA is 252 by 216 mils with 19 I/O and 6 power/ground leads. Also included were 27 test pads for prototype debug. The power consumption is 150 mW when enabled, and 20 mW when sleeping. Its primary function is to turn on and off a power metallic oxide semiconductor field-effect

transistor (MOSFET) in such a way that load current di/dt is controlled, and the MOSFET is protected from destructive fault conditions. Its secondary functions are to provide load voltage and load-current telemetry, overload status signals, and overload shut down for load fault current. The SCA requires five external capacitors, three of which are selectable for control of turn-off delay, current ramp rate, and overload delay. In Figure 1 there are four SCAs located in the center of the module, underneath the eight capacitors.

PASM Packaging Overview—The PASM uses the Lockheed Martin HDI packaging technology to fabricate a KAPTON™ (polyimide) -based multi-layer interconnect structure. The KAPTON™ structure is laminated one layer at a time to the top surface of the bare die, packaged parts and other active and passive components. Components may be mounted to the topmost layer of the HDI interconnect using standard surface-mount techniques. Components used in HDI are first characterized, which is the physical measurement of components and the mapping of component I/O locations for use during the generation of pads and traces. Pockets to accept the parts are machined into an alumina ceramic substrate (See Figure 5).

Pockets are sized to ensure that the topmost surface of the part is coplanar to the surface of the substrate. The substrate is patterned by sputter deposition, photolithography, and etching to form the required elements prior to component placement (See Figure 6).

The die is attached with thermoplastic resin, thermosetting epoxies (conductive and non-conductive) and various high temperature solders (See Figure 7).

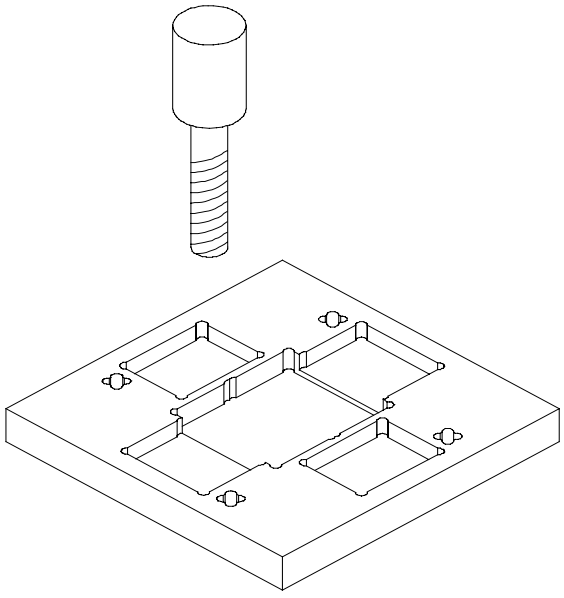

Figure 5. Ceramic Substrate Milling

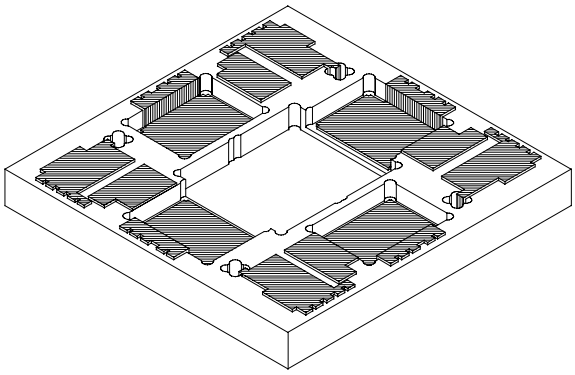

Figure 6. Substrate Masking and Metallization

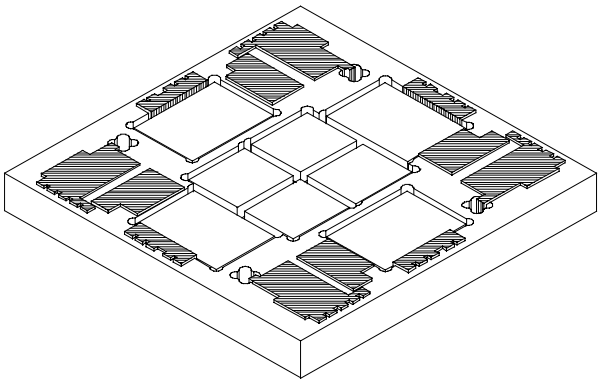

Figure 7. Populating and Bonding Parts

The interconnect layer is fabricated upon the populated substrate as follows:

Using a combination of vacuum, heat, and pressure a KAPTON™ film is laminated onto the populated substrate using thermoplastic adhesive. The interconnect bond pads are located using an image processing system. A direct-write laser forms vias through the KAPTON™ to the interconnect bond pads and to I/O pads on the substrate metallization.

The first interconnect layer is formed by sputtering films of titanium, copper, and titanium again. The metals are patterned by exposing a negative photo-resist with a direct-write, computer-controlled laser. The metal is then chemically etched leaving the desired circuit pattern (See Figure 8).

Subsequent layers are formed by laminating additional layers of KAPTON™ onto the substrate using a thermosetting adhesive and repeating the drill, metallization, pattern, and etch process. The module is then populated with surface-mounted components (See Figure 9).

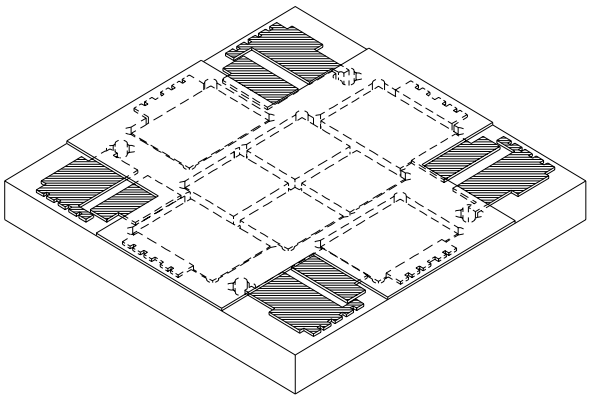

Figure 8. HDI Laminating and Etching

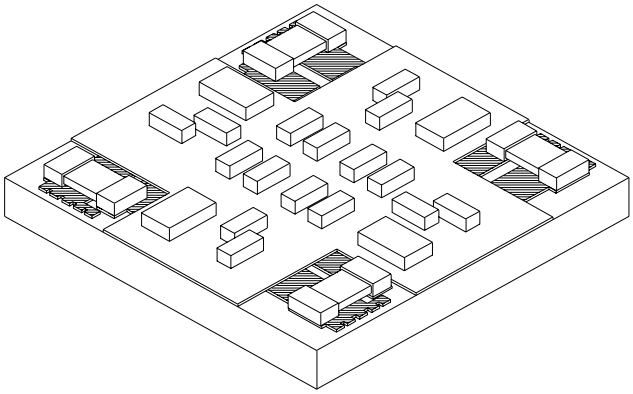

Figure 9. Attaching Surface-Mounted Parts

The completed HDI module is epoxy-bonded into a standard KOVAR™ package and the I/O is wire-bonded (See Figure 10). The package is seam-sealed to complete the module assembly.

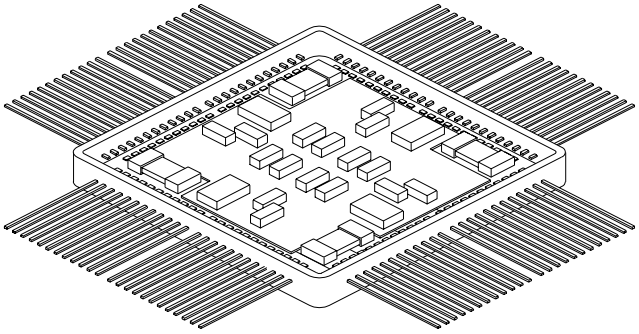

Figure 10. Wire-Bonding I/O Leads

Multi-chip module packaging issues—PASM presented three major design issues: current handling capacity of multi-layer thin-film HDI structure, heat dissipation, and CTE (coefficient of thermal expansion) mismatch of large power die-to-substrate. The current handling capacity of HDI in this application was less of a concern than the "ON" resistance of the switch. The minimization of "ON" resistance was a critical performance characteristic, if the switch was to perform properly as a primary as well as a secondary side or conditioned power switch. The trace size required to carry the specified current with a maximum 10° C rise using 15-µm copper is approximately 0.3-in. wide. The switch FET die is 0.366 by 0.266 in., which means the trace-width requirement is nearly the length of the FET die. The required trace width indicated that the switch FET must lie parallel to the package interconnect to provide adequate trace access to package input/output pins. The FET die must also be physically next to package output to limit total interconnect length (i.e., lead length, package I/O wire bonds, and HDI interconnect).

Thermal dissipation in the PASM for normal steady state conditions at 3-A maximum-rated current on all four switches was not a significant design driver due to the thermally efficient "chips first" HDI packaging as well as physically large FET die used for switching. The normal operation of the PASM with all four switches in use results in the FET die temperature approximately 4.0° C above ambient.

The real design concern was "failure" operation of the PASM. The PASM is designed to be a smart switch: that is, respond to a current over a specified limit. If a load controlled by the PASM exceeds a preset current for a specified time, the PASM quickly shuts off. The affected load is protected and the failure is prevented from propagating. The PASM is designed to handle large transient currents, shut off, and be available to be commanded back on when required.

The current available from most spacecraft power sub-systems in short circuit condition is extremely large. PASM is designed to survive large current transients and turn off without being damaged or damaging the surrounding switches contained in the module. Thermal analysis of the PASM switch components was performed using SINDA 87™ assuming an ambient temperature of 75° C. Electrical power applied to each junction in the switch was modeled as a square wave pulse of 100-µsec duration. Only the FET had a significant junction temperature increase from the initial 75° C ambient. Results of the transient model are tabulated in Table 2.

The CTE differences between the large FET and the 96% alumina substrate typically used for HDI was evaluated to insure the product would meet mission requirements. The large size of the FET die in the PASM required the use of gold-clad-molybdenum tabs (molytab) or interposers between the base of the FET and the alumina substrate [4]. The FET-die-to-molytab attachment used gold/germanium eutectic; the molytab-to-substrate attachment used Indalloy™ 165 eutectic. The use of the molytab in this

application was dictated by (1) the physical size of the die, (2) the large number of possible thermal and power cycles the module would be exposed to in normal operation, and (3) the inability to use a silver-loaded epoxy.

Table 2. Transient Thermal Analysis*

Component	Power (W)	$T_{junction}$ (C)
Q1 (FET)	3500	96.2
CR1	0	77.0
U1 (ASIC)	0.151	75.0
R1 (Current Sense)	290	75.6
Q31	0.370	75.7**

* One Switch circuit consists of Q,CR,U, and R (Capacitors not shown).
** Q31 is an Adjacent FET, Normal Operation (Shown for Comparison).

The design of power electronics is constantly under pressure to reduce size and weight and increase interconnect density to better integrate power products with the end users they serve. The drive to integrate power electronics generally requires technologies that do not easily lend themselves to carrying large currents. The Lockheed Martin HDI technology provides a unique blend of capabilities for power packaging. HDI technology has historically been used for digital or RF applications and has only been applied to power packaging in the last few years. The standard HDI process has been modified to allow use of up to 24 µm (0.001 in.) copper layers for power applications. Processing temperatures have been decreased to allow the use of magnetic as well as packaged parts.

Accommodation of PASM on DS1—A set of PASMs was launched on DS1 in October 1998 for flight-performance verification and validation. The DS1 PASMs are mounted on a printed circuit board (see Figure 11) and housed in a VME cage. The outputs of the modules are connected to dummy loads for on/off characterization of the PASM switches and their performance evaluation during various phases of the mission. The first set of PASM performance test data from DS1 was received in February 1999.

2.5 Technology Interdependencies
PASMs were flown on DS1 as Category 3 electronics experiment and therefore had no direct impact on the performance of other technologies tested on DS1 or on other subsystems of the spacecraft.

2.6 Test Program
The test program included switching 5-V power to a 1-A resistive load through each of the eight switches (four per module). The switches were also operated in parallel (two at a time) to switch 5-V power to the same 1-A resistive load. Certain electrical design flaws in the switch control ASICs prevented them from operating completely. As a result, the in-rush and fault isolation features of the PASM switches were not tested.

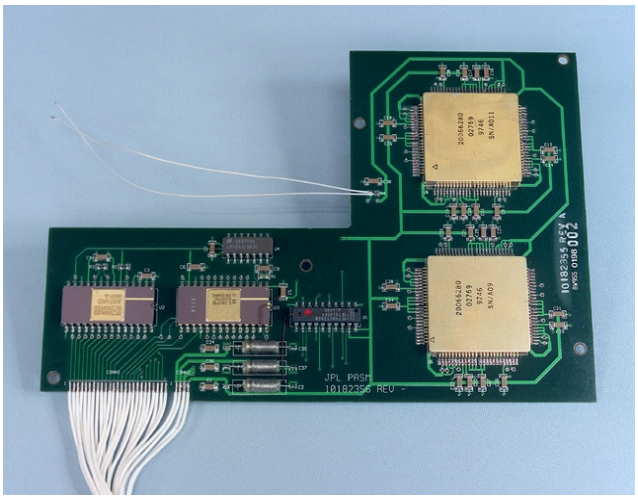

Figure 11. PASM DS1 Flight Configuration

2.7 Comparison Between Ground Test and Flight Test
Figures 12 and 13 show the PASM in-orbit performance over time. Figure 12 shows the load current supplied by each of the eight PASM switches, and Figure 13 shows the voltage at the load supplied by the individual switches. These figures show that over a period of nearly 8 months, all eight switches performed satisfactorily and did not exhibit any degradation in the performance, primarily in terms of the excessive voltage drop in the switch itself. No difference was seen in the PASM ground and in-orbit performance.

3.0 Technology Validation Summary

A state-of-the-art PASM using HDI and mixed signal ASIC technologies has been developed. This program has significantly contributed in validating several production processes which are key to the development and production of future high-density lightweight power electronics. The eventual goal is a self-contained, three-dimensional avionics module for both space and commercial applications.

The PASM performance test data received from the DS1 flight and incorporation of various lessons learned from the design and fabrication phase of this module should help in enhancing the performance of the second generation PASM currently under development.

NASA/JPL has recently awarded a second contract to the Boeing Company to produce a second-generation ASIC to correct the previous design flaws and simplify the design. These second-generation ASICs will be used in PASMs being procured for the X2000 program.

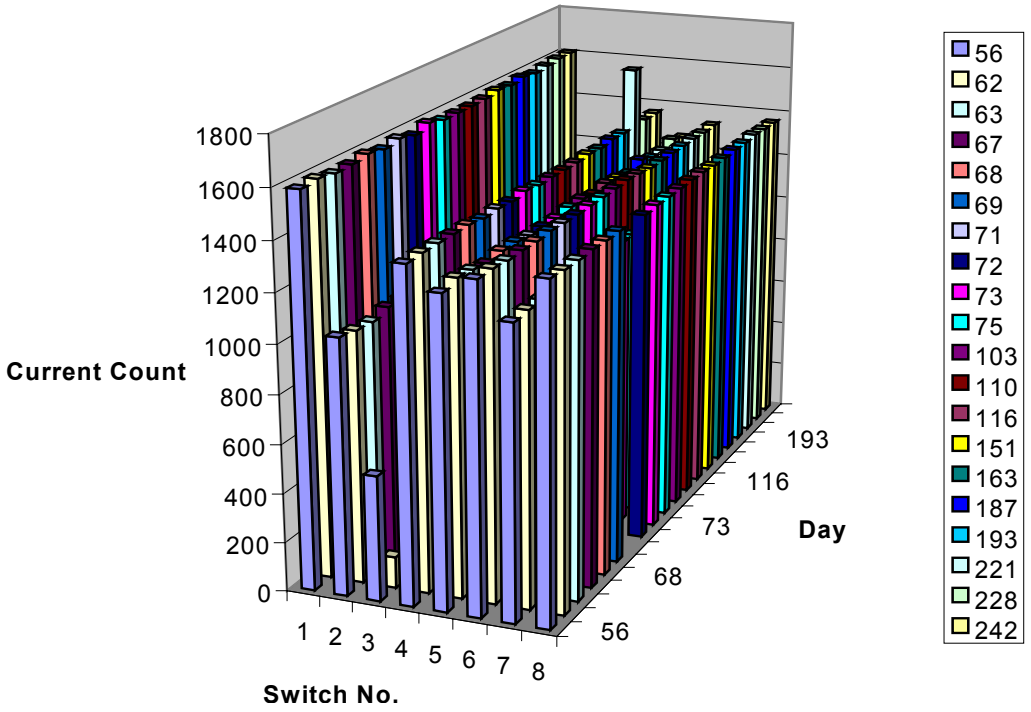

Figure 12. PASM Flight Performance (Switched Current vs. Time)

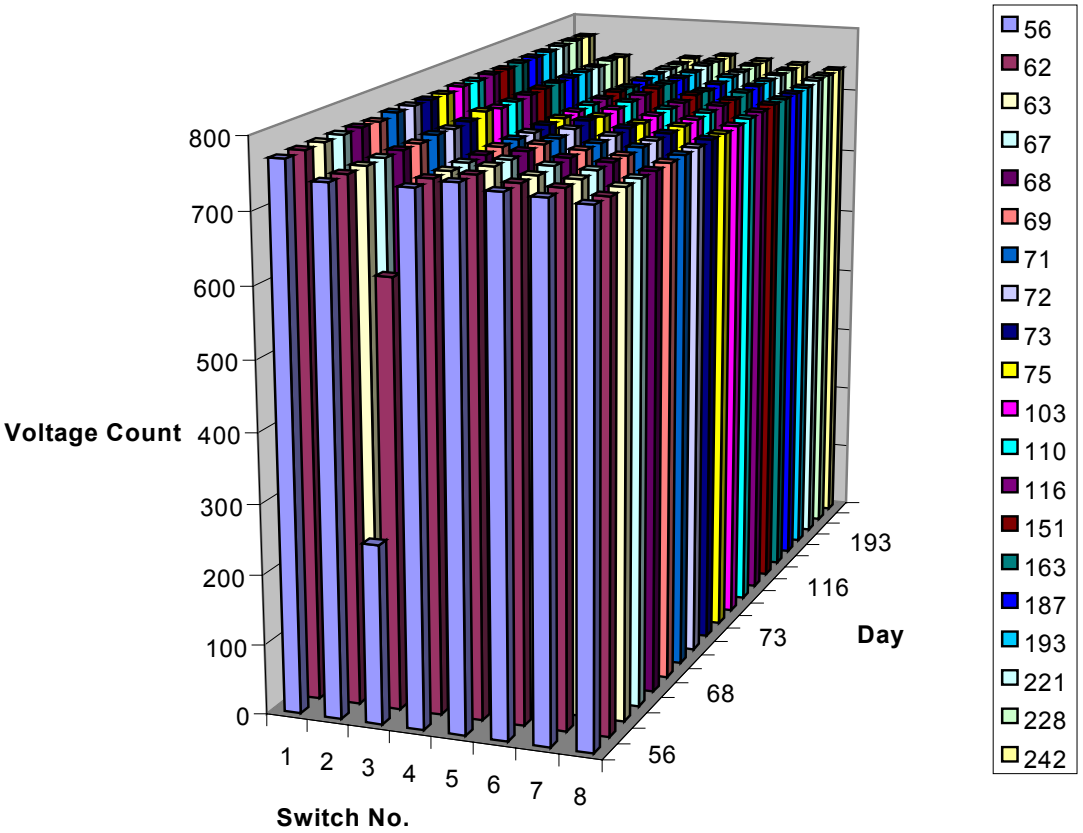

Figure 13. PASM Flight Performance (Switched Voltage vs. Time)

4.0 Technology Application For Future Missions

The PASM, as well as the technologies used in building the PASM, have succeeded to a large extent in satisfying NASA's goal of miniaturizing power electronics and have a added wide-ranging applicability to future NASA science missions as well as other LEO and GEO spacecraft. Lockheed Martin was recently awarded a $16 million contract to design and build multiple dc-dc converters, shunt regulator modules, and lithium-ion battery chargers using PASM technologies. Supply of a large number of second-generation PASMs is also included in the same contract for NASA's X2000 programs. Figure 14 shows the technology road map for the recently awarded contract and the future product development possibilities.

The PASM design and its technologies are also applicable to consumer electronics—power-switching applications that always emphasize miniaturization and lightweight products.

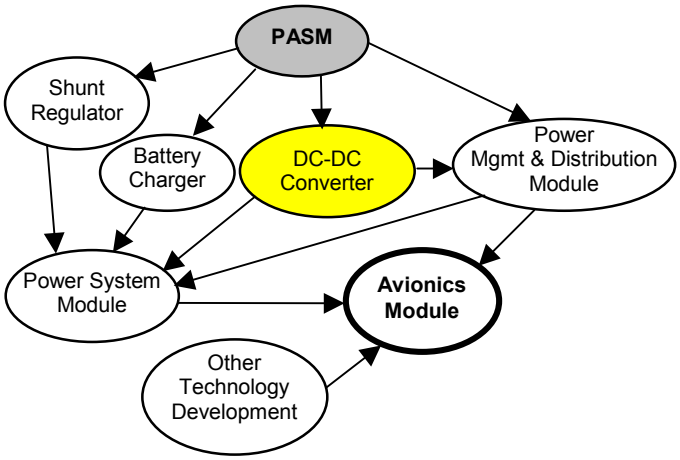

Figure 14. Future HDI Technology Product Road Map

5.0 Acknowledgments

The work described in this report was carried out at Lockheed Martin Communications and Power Center, Newtown, Pennsylvania; Lockheed Martin Government Electronics, Morrestown, New Jersey; and at the Boeing Company, Seattle, Washington. The financial support for the design and development of the PASM and its ASICs was provided by Lockheed Martin and the Boeing Company. The program to develop the PASM was organized by JPL for the National Aeronautics and Space Administration, which also paid for its fabrication, test and flight validation on DS1.

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Appendix A. DS1 Technology Validation Telemetry Channels

Below is a list of all of the telemetry channels that the PASM team collects and uses. (Kirk Fleming, 10/14/99.)

Channel	Mnemonic
P-0315	PASMdataQual
P-0316	PASMdataWord
P-0317	PASM_t_stam;
B-0032	bmPASMgdcdct
B-0033	bmPASMbdcdct
B-0034	bmPASMbdtlct

Appendix B. DS1 Technology Validation Power on/off Times

LPE/PASM initial turn-on was February 25, 1999. The experiment was then conducted weekly from power-off. (Kirk Fleming, 10/29/99)